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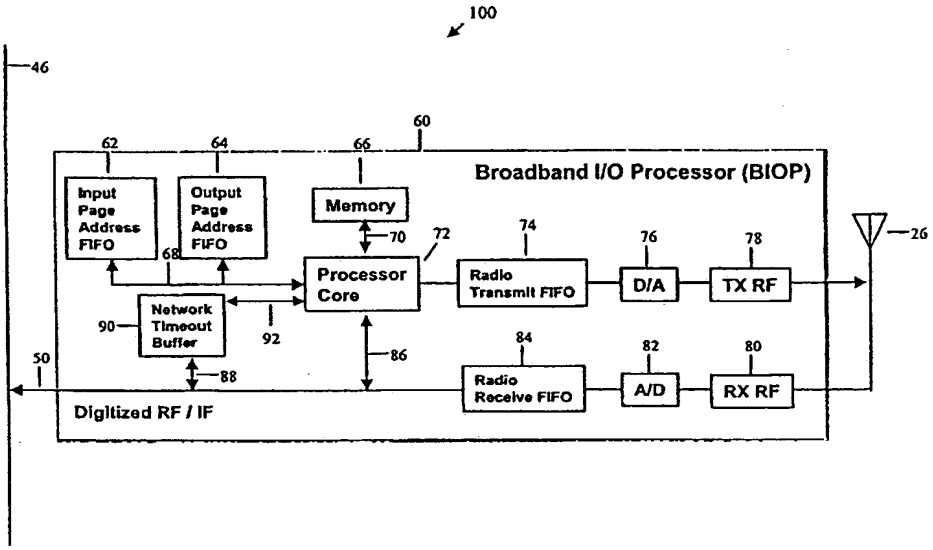
(54) Title: PROGRAMMABLE BROADBAND INPUT/OUTPUT PROCESSOR



(57) Abstract

A programmable broadband input/output processor (60) includes a memory (66) to store configuration data, a radio receive First–In–First–Out circuit (84), and a radio transmit First–In–First–Out circuit (74). A processor core (72) is connected to the memory (66), the radio receive First–In–First–Out circuit (84), and the radio transmit First–In–First–Out circuit (74). The processor core (72) selectively receives subsets of the configuration data based upon parameters associated with data in the radio receive First–In–First–Out circuit (84) and the radio transmit First–In–First–Out circuit (74). Page address First–In–First–Out circuits (62, 64) are also connected to the processor core (72). A communication bus (46) connected to the processor core (72) selectively relays control information to and from a central site station (42).

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PROGRAMMABLE BROADBAND INPUT/OUTPUT PROCESSOR

This application claims priority to the provisional patent application entitled, "Programmable Broadband Input/Output Processor", Serial Number 60/133,139, filed May 7, 1999.

BRIEF DESCRIPTION OF THE INVENTION

This invention relates generally to digital communications. More particularly, this invention relates to a technique for broadband input/output processing that facilitates the remote reconfiguration of digital information devices.

BACKGROUND OF THE INVENTION

As the need for flexibility increases in wireless and wireline systems, it is increasingly important to support high throughput input/output. High throughput input/output is especially important to enable a software-programmable, hardware-reconfigurable product platform. Support for high throughput input/output is critical for infrastructure products, such as base stations in cellular applications and sever sites in cable and remote access systems.

Figure 1 illustrates a prior art cellular communications network 20. Each base station 22 includes an antenna 26, an RF transceiver 28 for frequency up- and down-conversion, and a plurality of baseband modems 30. In transmit mode, the modems 30 accept digital baseband information from the system bus 24 via interface 32, and perform the necessary channelization, modulation and other signal processing. The RF transceiver 28 then performs frequency upconversion and power amplification. In

receive mode, the RF transceiver 28 performs amplification, filtering and downconversion, while the modems 30 perform demodulation and dechannelization, and output the recovered digital data (information) to system bus 24 via interface 32. The RF transceiver 28 must operate separately on each of a plurality of bands of interest, while the modems 30 must be replicated once for each RF band of interest. Thus, prior art systems have a relatively large number of devices (e.g., modems) distributed throughout the network, making centralized control and repair difficult.

In view of the foregoing, it would be highly desirable to provide an improved communication network to facilitate enhancements in input/output processing in broadband devices.

SUMMARY OF THE INVENTION

A programmable broadband input/output processor includes a memory to store configuration data, a radio receive First-In-First-Out circuit, and a radio transmit First-In-First-Out circuit. A processor core is connected to the memory, the radio receive First-In-First-Out circuit, and the radio transmit First-In-First-Out circuit. The processor core selectively receives subsets of the configuration data based upon parameters associated with data in the radio receive First-In-First-Out circuit and the radio transmit First-In-First-Out circuit. Page address First-In-First-Out circuits are also connected to the processor core. A communications bus connected to the processor core selectively relays control information to and from a central site station.

The invention provides a flexible communications gateway in high-throughput signal processing systems. More particularly, the invention provides a programmable device to perform communications between radio outputs and central processing modem pools. The modular architecture of the invention reduces the number of individual channel cards required in wired or wireless infrastructure products. The programmability associated with the invention facilitates a single hardware platform to be configured for multiple communication bus standards and multiple analog-to-digital front-ends. Further, the invention provides flexible data communications management capability via a programmable data gateway to central site pools.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention, reference should be made to the following detailed description taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a prior art cellular communications network.

FIGURE 2 illustrates a cellular communications network constructed in accordance with an embodiment of the invention.

FIGURE 3 illustrates a broadband input/output processor constructed in accordance with an embodiment of the invention.

Like reference numerals refer to corresponding parts throughout the drawings.

DETAILED DESCRIPTION OF THE INVENTION

Figure 2 illustrates an improved cellular communications network 40 constructed in accordance with an embodiment of the invention. In Figure 2, the individual base stations 48 each employ a single broadband I/O processor (BIOP). Furthermore, all signal processing modems are co-located in the central site station 42. In transmit mode, the BIOP accepts digitized RF or IF signals from the high-speed system bus 46, converts the digitized signal into a broadband analog RF signal, and delivers the broadband RF signal to the antenna 26. In general, the broadband RF signal includes all individual RF bands of interest. In receive mode, The BIOP accepts the entire / overall RF or IF frequency band of interest, digitizes the in-band information, and delivers the digitized information to system bus 46. The BIOPs at the base stations 48 can be remotely configured by the central site station 42 via the system bus 46 and interface 50. System bus 46 may be implemented according to any standard private or virtual private network that meets minimum quality-of-service requirements. As a benefit, the co-located pool of modems can be serviced and/or reconfigured much more expeditiously, since they are not physically distributed across the base stations. This configuration also simplifies the architecture of the base stations.

Figure 3 illustrates a broadband input/output processor 60 constructed in accordance with an embodiment of the invention. The processor 60 includes a receive RF subsystem (RX RF) 80 which performs RF amplification and, optionally, block

downconversion to IF. Processor 60 also includes an analog-to-digital converter 82 which receives an incoming radio frequency signal. The analog-to-digital converter 82 outputs a digital signal to a radio receive First-In-First-Out (FIFO) 84.

Analogous functionality is provided at the transmission port of the processor 60. In particular, a radio transmit FIFO 74 routes a digital signal to a digital-to-analog converter 76. The digital-to-analog converter 76 produces an analog signal that is transmitted in conjunction with power amplifier 78 in a conventional manner.

Figure 3 also illustrates a broadband input/output processor core 72. The core 72 may be implemented with a microprocessor, a digital signal processor, an FPGA, a PLA, a PLD, a CPLD, a Gate Array, or an ASIC. The core 72 accesses a memory 66, which contains configuration code that enables the core to be programmed to support different wireless standards and services.

The core 72 is also linked to an output page address FIFO 64 and an input page address FIFO 62. Further, the core 72 is connected to a network timeout buffer 90. A communication bus 50 connects the processor 60 to central site station 42 via bus 46.

The core 72 operates in two modes simultaneously. The core 72 is generally under the control of an operating system, either locally or at the central site station 42.

In a first mode of operation, the core 72 operates in a radio receive mode. The core 72 accesses the FIFO 84. The FIFO accommodates the typically bursty nature (variable rate input/output (I/O)) of reads/writes to the communication bus 46. The core 72 configures itself according to which band it is receiving data from in the FIFO, and which central site processing station this data is destined for. Based upon these two parameters, the core 72 downloads the configuration code from memory 66. The configuration code enables the reading of data in the correct format from the FIFO and sets up the transmission format to enable the data to be placed on the communications bus 46 using the proper protocol. To read the data in the correct format out of the FIFO 84, the configuration code must note the sampling rate, the sample word length, and the frame length. To prepare the transmission format for the communications bus 46, the configuration code must note the protocol format, the parameters for the protocol (e.g., block size, timeout duration, ACK/NACK, etc.) and any error-recovery procedures. The Page Address FIFOs 62, 64 hold the physical page addresses associated with buffers in virtual memory located at the central site processing station.

At the end of a page transfer, the core 72 reads the next address from the head of the appropriate Page Address FIFO and begins transferring data to it. The core 72 triggers an interrupt when the supply of page addresses runs low. Servicing this interrupt in a timely manner is critical, and is the responsibility of the operating system at the central site processing station. The network timeout buffer is used to store the last N packets of data sent over the bus as an error-recovery measure.

A second mode of operation is the radio transmit mode. The inputs from the central site processing station are read according to the configuration the core 72 downloads from memory 66. Again, this configuration determines the data format for the data to be read and pumped to the radio transmit FIFO 74 as well as the protocol to use to format communications over the bus 46 and with the central site processing station 42. The page address FIFOs 62, 64 are used by the core 72 to read the radio transmit data from the correct virtual memory location using the communications bus. The protocol for communication is found in the configuration file for the core 72. To read the data in the correct format from the location in virtual memory, the configuration code must note the parameters for the protocol (e.g., block size, timeout duration, ACK/NACK, etc.) and any error-recovery procedures. To prepare the transmission format for the radio transmit FIFO 74, the configuration code must note the protocol format, the sampling rate, the sample word length, and the frame length. The page address FIFOs 62, 64 hold the physical page addresses associated with buffers in virtual memory located at the central site processing station 42. At the end of a page transfer, the core 72 reads the next address from the head of the appropriate page address FIFO and begins transferring from it. The core 72 triggers an interrupt when the supply of page addresses runs low. Again, servicing this interrupt in a timely manner is critical, and is the responsibility of the operating system at the central site processing station 42. The network timeout buffer may or may not be used in the radio transmit mode.

The core 72 must be programmable in that it can be either software configurable or hardware reconfigurable. This allows the storing of configuration information in memory, and the download of this information into the core 72 creates the capability to be a programmable input/output processor.

At the end of a page transfer, the core 72 reads the next address from the head of the appropriate Page Address FIFO and begins transferring data to it. The core 72 triggers an interrupt when the supply of page addresses runs low. Servicing this interrupt in a timely manner is critical, and is the responsibility of the operating system at the central site processing station. The network timeout buffer is used to store the last N packets of data sent over the bus as an error-recovery measure.

A second mode of operation is the radio transmit mode. The inputs from the central site processing station are read according to the configuration the core 72 downloads from memory 66. Again, this configuration determines the data format for the data to be read and pumped to the radio transmit FIFO 74 as well as the protocol to use to format communications over the bus 46 and with the central site processing station 42. The page address FIFOs 62, 64 are used by the core 72 to read the radio transmit data from the correct virtual memory location using the communications bus. The protocol for communication is found in the configuration file for the core 72. To read the data in the correct format from the location in virtual memory, the configuration code must note the parameters for the protocol (e.g., block size, timeout duration, ACK/NACK, etc.) and any error-recovery procedures. To prepare the transmission format for the radio transmit FIFO 74, the configuration code must note the protocol format, the sampling rate, the sample word length, and the frame length. The page address FIFOs 62, 64 hold the physical page addresses associated with buffers in virtual memory located at the central site processing station 42. At the end of a page transfer, the core 72 reads the next address from the head of the appropriate page address FIFO and begins transferring from it. The core 72 triggers an interrupt when the supply of page addresses runs low. Again, servicing this interrupt in a timely manner is critical, and is the responsibility of the operating system at the central site processing station 42. The network timeout buffer may or may not be used in the radio transmit mode.

The core 72 must be programmable in that it can be either software configurable or hardware reconfigurable. This allows the storing of configuration information in memory, and the download of this information into the core 72 creates the capability to be a programmable input/output processor.

The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the specific details are not required in order to practice the invention. In other instances, well-known circuits and devices are shown in block diagram form in order to avoid unnecessary distraction from the underlying invention. Thus, the foregoing descriptions of specific embodiments of the present invention are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed; obviously many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalents.

IN THE CLAIMS:

1. A programmable broadband input/output processor, comprising:

a memory to store configuration data;

a radio receive First-In-First-Out circuit;

a radio transmit First-In-First-Out circuit;

a processor core coupled to said memory, said radio receive First-In-First-Out circuit, and said radio transmit First-In-First-Out circuit to selectively receive sub-sets of said configuration data based upon parameters associated with data in said radio receive First-In-First-Out circuit and said radio transmit First-In-First-Out circuit; and

a communications bus connected to said processor core to selectively relay control information to and from a central site station.

2. The programmable broadband input/output processor of claim 1 further comprising page address First-In-First-Out circuits connected to said processor core.

3. The programmable broadband input/output processor of claim 1 further comprising a network timeout buffer connected to said processor core.

4. A communications network, comprising:

a central site station storing a plurality of communications modems; and

a plurality of base stations, each base station of said plurality of base stations including

a memory to store configuration data;

a radio receive First-In-First-Out circuit;

a radio transmit First-In-First-Out circuit;

a processor core coupled to said memory, said radio receive First-In-First-Out circuit, and said radio transmit First-In-First-Out circuit to selectively receive sub-sets of said configuration data based upon parameters associated with data in said radio receive First-In-First-Out circuit and said radio transmit First-In-First-Out circuit; and

a communications bus connected to said processor core to selectively relay control information to and from said central site station.

5. The communications network of claim 4 wherein each base station further comprises page address First-In-First-Out circuits connected to said processor core.

6. The communications network of claim 4 wherein each base station further comprises a network timeout buffer connected to said processor core.

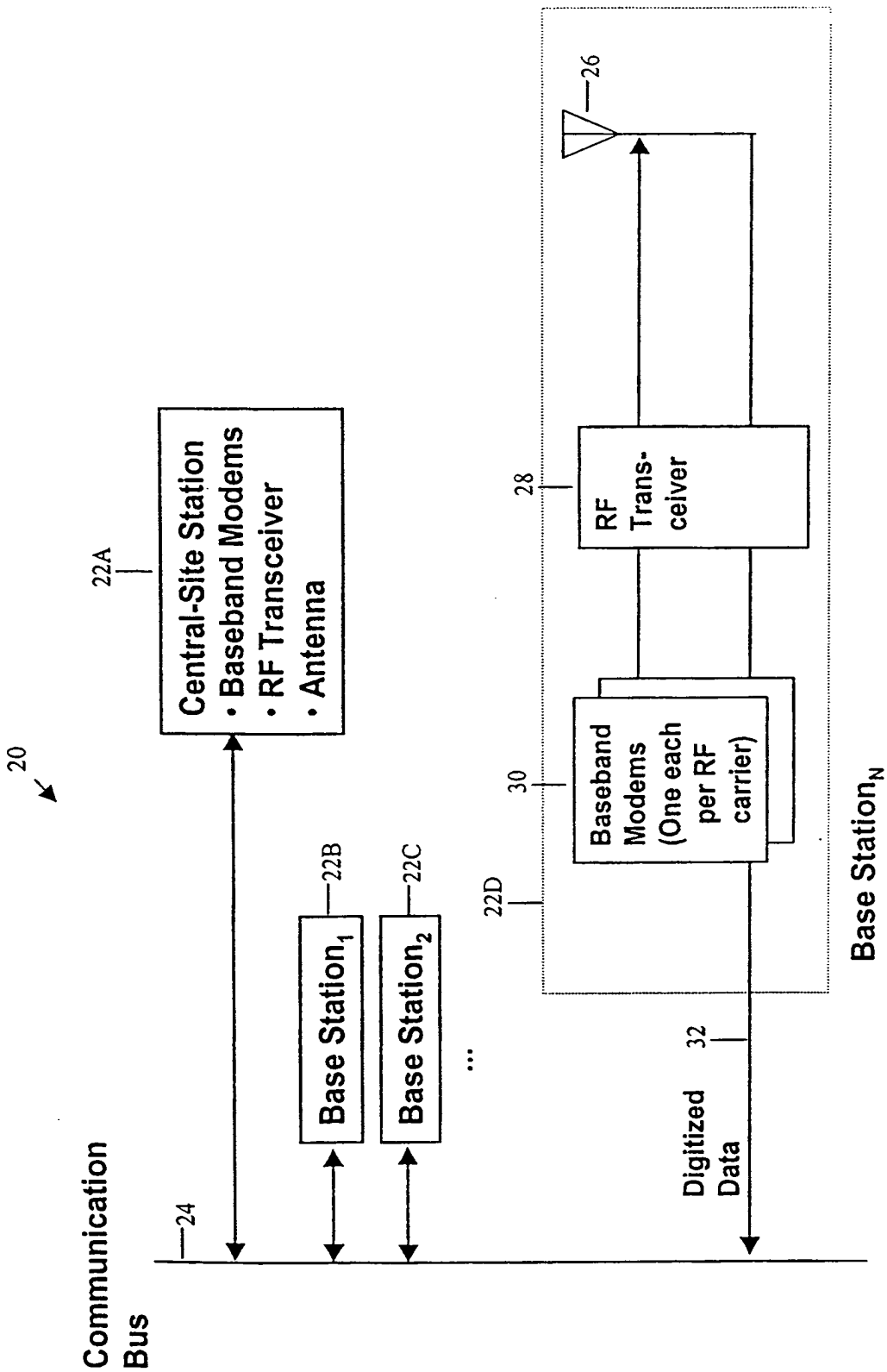

Fig. 1
(Prior Art)

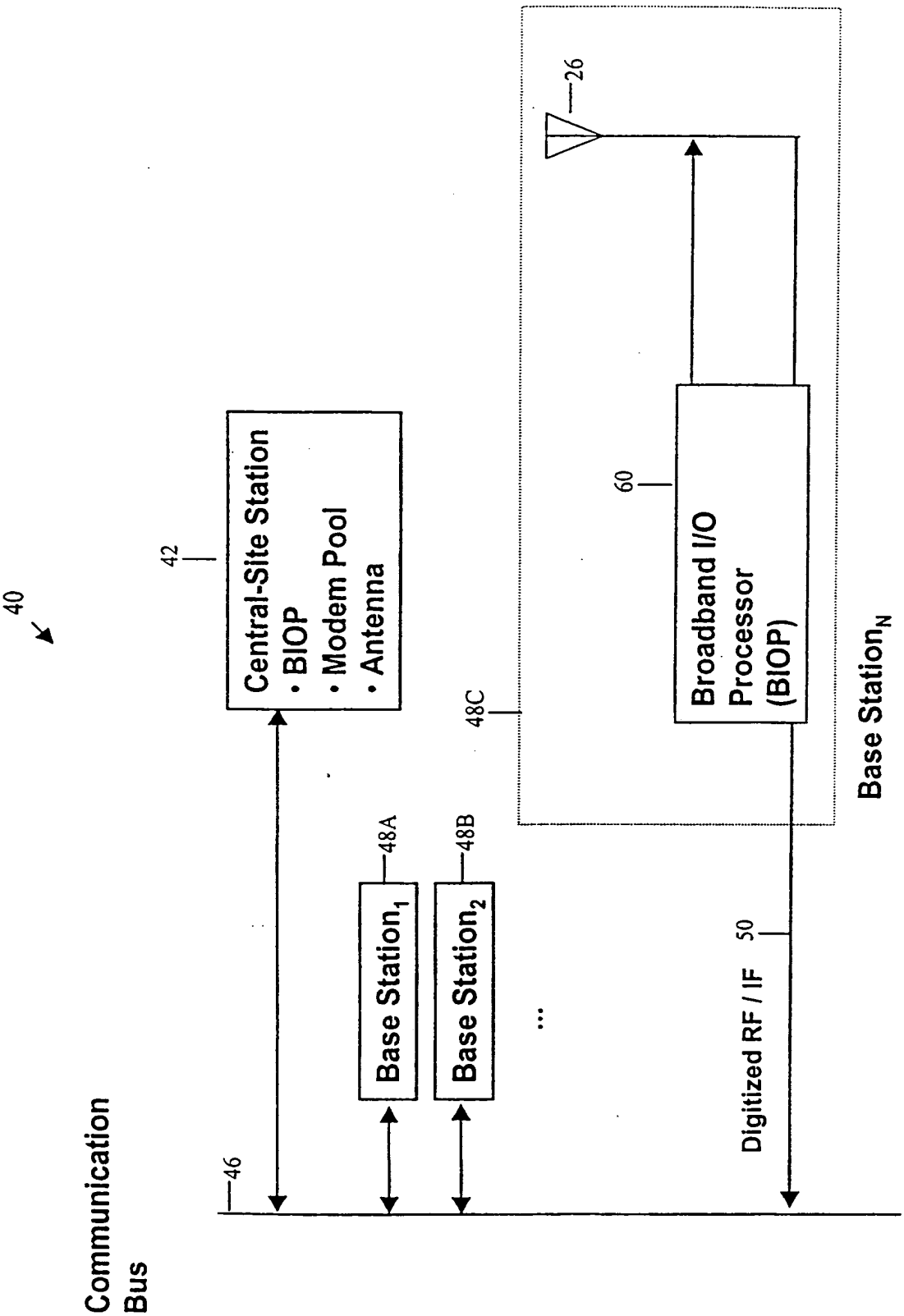
40
42
Central-Site Station
• BIOP
• Modem Pool
• Antenna
26
60
Broadband I/O
Processor
(BIOP)
48C
Base Station$_N$
48A
Base Station$_1$
48B
Base Station$_2$
...
50
Digitized RF / IF
46
Communication
Bus

Fig. 2

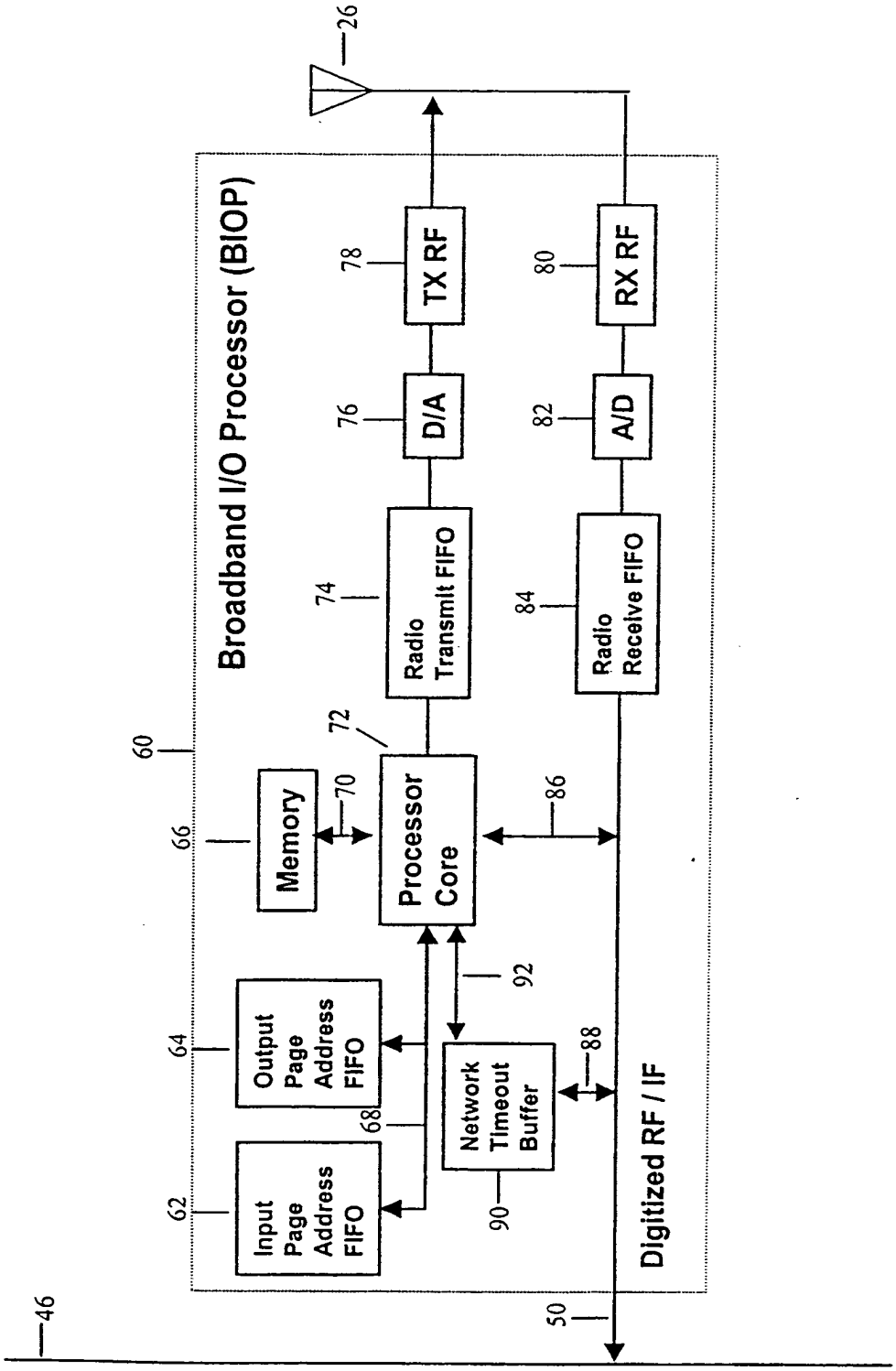

Fig. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/12476

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) :G06F 13/10, 15/177
US CL :340/825.06, 825.15; 455/419, 420; 709/221; 710/8, 10, 11
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 340/825.06, 825.15; 455/419, 420; 709/221; 710/8, 10, 11

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WEST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,625,627 A (ISHI) 29 April 1997, fig. 10, col. 13, lines 41-49.	1-6
Y	US 5,822,273 A (BARY et al) 13 October 1998, col. 5, lines 12-17, col. 9, lines 51-67, col. 10, lines 12-45	1-6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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